REMARKS

The Examiner's action mailed on September 11, 2003 has been received and its contents carefully considered.

Claims 1-5 are pending in this application. Claims 1, 4 and 5 are amended and new claims 6-20 are added herein. Amended claim 1 and new claims 6 and 14 are independent claims.

In the Action, the Examiner objects to title of the invention as not being descriptive, and to the abstract of the disclosure as containing a minor typographical error. The Examiner is respectfully requested to review the amended title and amended abstract, and withdraw the objections thereto.

Claims 4 and 5 stand rejected under USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the Examiner asserts that the limitation "said pulse transfer circuit," in claim 4, and the limitation "the signal," in claim 5, lack sufficient antecedent basis. Claims 4 and 5 have been amended in response to the Examiner's concerns. The Examiner is respectfully requested to review the amended claims and withdraw the §112, second paragraph, rejections.

Applicant notes with appreciation in the Examiner is early indication that claim 5 would be allowable if rewritten to overcome the rejection under 35 USC §112, second paragraph, set forth in the Office Action and to include all the limitations of the basic claim and any intervening claims.

Claims 1-4 stand rejected under USC section 102(e) as being anticipated by Tobita et al. (U.S. Patent No. 6,385,257). Claim 1 is amended herein to more clearly distinguish over the Tobita reference.

Regarding claim 1, the Examiner points to Tobita as disclosing a receiving circuit (Figure 1) comprising: a demodulator which demodulates the received signal (Figure 1, item 55) and outputs the demodulated data therefrom; a detector which detects a synchronizing pattern (Figure 10, item 64) included in the demodulated data and outputs an instruction signal for providing instruction for the result the result of detection (Figure 10, item CK24); a pulse generator (Figure 12) capable of receiving the instruction signal

(Figure 12, item CK24) and outputting a pulse signal (Figure 12, item ADM) each time a predetermined time lapses since the reception of the instruction signal (figure 12, ADM based on window pulse generator 104 and clock); a control circuit (Figure 12, item 102) which outputs control signals corresponding to at least either one of the instruction signal and the pulse signal (Figure 12, outputs based on CK24); and a clock generator which generates a clock signal for storing and outputting desired data (Figures 1, 10, 12 and others; various components store and output) included in the demodulated data in response to the control signal (Figure 10, output of 64a generates a clock CK24 which is used by other components for this purpose).

The present invention is directed to a receiving circuit suitable for use in a radio apparatus operating in TDMA mode, in which burst signals each containing a synchronization pattern and data are received in predetermined time slots (see, generally, application pages 1-2). In contrast, Tobita is directed to a frequency demodulating circuit for demodulating a frequency-modulated signal expressing digital data in an optical disk apparatus (Tobita abstract; column 1, lines 14-15). Tobita fails entirely to teach or suggest "a demodulator circuit demodulating a radio signal that includes a burst signal and outputting the demodulated data therefrom" (emphasis added) as amended claim 1 recites. Item 55 of Figure 1, to which the Examiner refers, is described in Tobita as a modulator, rather than a demodulator. Figure 1 does show a data demodulator 59, which executes an NRZI inverse-conversion process on reproduction data Dp (column 12, lines 60-61), but clearly, this is not at all comparable to the function of the demodulator recited in claim 1.

Other elements identified by the Examiner in Tobita also failed to correspond to those recited in the claims. For example, item 64 in Figure 10 is identified in Tobita as a phase locked loop (PLL) circuit comprising a voltage controlled oscillator 64a, a frequency divider 64b, a phase comparator 64c, and a low-pass filter 64d (column 13, lines 23-33), and does not correspond at all to a "detector which detects a synchronizing pattern included in the demodulated data", as recited in claim 1. Item CK24, which the Examiner asserts corresponds to the recited instruction signal, is in fact a clock signal output from the voltage controlled oscillator 64a, and item ADM, which Examiner asserts corresponds the recited pulse signal output from the recited pulse generator, is identified instead as address

information derived by the ADIP decoders 60 from the digital data read from the optical disk (column 13, lines 34-45).

In general, the art disclosed in Tobita is not analogous to that of the present invention and, therefore, not applicable as the basis of a prior art rejection. Accordingly, it is respectfully submitted that amended claim 1, as well as claims 2-5, patentably distinguish over the applied prior art.

New claims 6-20 are added to afford additional patent protection for the invention disclosed in the application. It should be clear from the preceding discussion that the new claims also distinguish over the applied art.

All of the objections and claim rejections having been addressed, it is respectfully submitted that the application, as amended, is in condition for allowance. Notice of such, with claims 1-20, is earnestly solicited.

Should the Examiner believes that an interview would be helpful in resolving any open issues regarding this application, the Examiner is respectfully invited to call the undersigned attorney to schedule such an interview.

Respectfully submitted,

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Date

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Attachment:
Amended Abstract

A2

ABSTRACT OF THE DISCLOSURE

A pulse generator is provided which operates as a counter capable of resetting a count according to an instruction signal for providing instructions for the detection of a synchronizing pattern from a ~~previously-received~~ previously received burst signal having some of continuous pseudo random patterns. The pulse generator performs counting up to timing provided to detect a synchronizing pattern of a burst signal having a continuous part of a pseudo random pattern to be consecutively received and thereby outputs a count-up signal CO similar to the instruction signal.